

# Dr. rer. nat. Jörg Brauer

## Contact



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*"Luck favors the prepared mind."*  
Louis Pasteur, 1822-1895

## About me

I moved to Bremen.

Prior to moving up north, I used to be a PhD student heading the [\[mc\]square](#) project. [mc]square is a verification platform for microcontroller binary code. The key idea in [mc]square is to combine different formal methods in order to analyze hardware-specific microcontroller code. My own focus is the development of static analysis and abstract interpretation techniques specifically suited for verifying bit-twiddling programs. I am also involved in the [CEVTES](#) project, which is a joint project with the TU Vienna and the UAS Technikum Vienna on test-case generation for binary code.

Before I joined the Embedded Software Laboratory, I received my diploma degree from the Christian-Albrechts University of Kiel and visited [NICTA](#) in Sydney, Australia. At NICTA, I worked on [Goanna](#), a static analyzer for the C/C++ programming languages.

See [my CV](#) for more details.

## News

- **16/03/2012:** Today I had my last day in Aachen, I leave the Embedded Software Laboratory to work in industry.
- **06/03/2012:** The slides for my presentation on automatic abstraction at the [Compiler Design Lab](#) in Saarbrücken are available [here](#).
- **05/03/2012:** The slides for my talk at the Max-Planck Institute in Saarbrücken are available from [here](#).
- **01/03/2012:** The slides for my talk at [InBot'12](#) are available from [here](#).
- **24/01/2012:** The paper [Inferring Definite Counterexamples Through Under-Approximation](#),

- which I co-authored with [Axel Simon](#) from the TU Munich, was accepted to the [4th NASA Formal Methods Symposium \(NFM 2012\)](#).
- **22/11/2011:** I gave an invited talk at CEA, LIST in Paris about automatic generation of abstraction for binary code. The slides are available from [here](#).
  - **15/11/2011:** Today, I gave an invited talk about formal verification of PLC software at the University of Bremen. The slides are available from [here](#).
  - **03/11/2011:** I gave an invited talk on automatic abstraction for bit-vector relations at the TU Vienna and the IST Austria.
  - **01/09/2011:** I have received a best paper award from [FMICS'11](#) for the paper [Past Time LTL Runtime Verification for Microcontroller Binary Code](#). The paper was co-authored [Thomas Reinbacher](#), [Martin Horauer](#), [Andreas Steininger](#) and [Stefan Kowalewski](#).
  - **01/08/2011:** The paper *Automated Test-Trace Inspection for Microcontroller Binary Code* which I co-authored with [Thomas Reinbacher](#), [Daniel Schachinger](#) and [Andreas Steininger](#) from the TU Vienna as well as [Stefan Kowalewski](#) from our group was accepted to [RV'11](#).
  - **20/07/2011:** The implementation for my [CAV'11 paper](#) is available from <http://www.cs.kent.ac.uk/amkdistribution>.
  - **03/07/2011:** The paper *Precise Control Flow Reconstruction Using Boolean Logic* that I co-authored with [Thomas Reinbacher](#), my colleague from TU Vienna, has been accepted to [EMSOFT'11](#). In this paper, me and Thomas combine several techniques such as bit-blasting, my elimination algorithm from CAV and forward/backward analysis to compute fairly precise approximations of CFGs from binary code.
  - **01/07/2011:** The paper *Adaptable Value-Set Analysis for Low-Level Code* that I have co-authored with [René Rydhof Hansen](#), [Kim G. Larsen](#) and [Mads Chr. Olesen](#) from Aalborg University as well as [Stefan Kowalewski](#) from our department was accepted for presentation at [SSV'11](#).
  - **10/06/2011:** I was invited to give a talk at the [MT-LAB](#) meeting in Copenhagen. The MT-LAB is a Danish research centre for formal methods, and the talk was about my work on existential quantifier elimination.
  - **06/05/2011:** The paper [Past Time LTL Runtime Verification for Microcontroller Binary Code](#) that I have co-authored with [Thomas Reinbacher](#), [Martin Horauer](#), [Andreas Steininger](#) and [Stefan Kowalewski](#) was accepted for [FMICS'11](#). The workshop will be held in Trento, Italy around end of August.
  - **06/04/2011:** We have assembled a [programme committee](#) for [SSV 2011](#). Additionally, a call for papers is available [here](#).
  - **22/03/2011:** The paper [Existential Quantification as Incremental SAT](#) which I co-authored with [Andy King](#) and [Jael Kriener](#) was accepted for [CAV'11](#). Yeah!
  - **14/03/2011:** [SSV 2011](#) will be co-located with the [2nd Conference on Interactive Theorem Proving \(ITP\)](#) in Nijmegen, The Netherlands. ITP will take place from August 22 till August 25, and SSV will be held as a 2-day workshop starting the day thereafter.
  - **11/03/2011:** I will be visiting the group of [Kim G. Larsen](#) in Aalborg from April till June. Hence, if you need to contact me, please try via email.
  - **10/02/2011:** Together with [Marco Roveri](#) (FBK-IRST, Trento) and [Hendrik Tews](#) (TU Dresden), I will co-chair the [6th International Workshop on Systems Software Verification \(SSV 2011\)](#).
  - **09/02/2011:** My paper [Approximate Quantifier Elimination for Propositional Boolean Formulae](#) co-authored with [Andy King](#) was accepted for [NFM'11](#).
  - **07/12/2010:** My paper [Transfer Function Synthesis without Quantifier Elimination](#) co-authored with [Andy King](#) was accepted for [ESOP'11](#).
  - **28/10/2010:** Together with [Thomas Reinbacher](#), [Martin Horauer](#), [Andreas Steininger](#) and [Stefan Kowalewski](#), I received a best paper award for our contribution to [MEMICS'10](#).
  - **08/06/2010:** My paper [Range Analysis of Microcontroller Code using Bit-Level Congruences](#) co-

authored with [Andy King](#) and [Stefan Kowalewski](#) was accepted for [FMICS'10](#).

- **04/05/2010:** My paper [Automatic Abstraction for Intervals using Boolean Formulae](#) co-authored with [Andy King](#) was accepted for [SAS'10](#).

## Research Interests

- abstract interpretation of bit-vector programs (see [\[mc\]square](#)), in particular using *automatic abstraction*
- relational abstract domains
- formal verification
- software model checking
- software for embedded systems

In summary, I combine theoretical computer science with low-level programming, for example, by automatically deriving invariants for bit-twiddling binary code. I particularly enjoy utilizing SAT/SMT solvers for solving such problems. If you interested in this topic, you might want to check out [my SAS'10 paper](#) or [my ESOP'11 paper](#), which give a good feel about how precise SAT-based abstract interpretation of bit-vector programs (such as assembly code) can get. However, to make such techniques scale, you need to apply certain other techniques, such as the projection algorithm from [my CAV'11 paper](#).

## Professional Activities

- Symposium co-chair for the Symposium on Design & Verification Methodologies for Embedded Systems, which is a symposium within the IEEE/ASME International Conference on Mechatronic and Embedded Systems and Applications (MESA) 2012 in Suzhou, China.
- Co-chair of the [6th International Workshop on Systems Software Verification](#) (SSV 2011) in Nijmegen, The Netherlands.
- Co-chair for the 4th Symposium on Design & Verification Tools for Embedded Systems (DVTES 2011) at [IEEE/ASME International Conference on Mechatronic and Embedded Systems and Applications \(MESA\) 2011](#) in Washington DC, USA
- Program committee for the [15th International Workshop on Formal Methods for Industrial Critical Systems \(FMICS 2010\)](#) in Antwerp, Belgium
- Local organizer for the [4th International Workshop on Systems Software Verification \(SSV 2009\)](#) in Aachen, Germany

## B.Sc./M.Sc./Diploma Theses

We always have a number of different topics for diploma, bachelors, and masters theses in the [\[mc\]square](#) project. Even though I do not supervise theses myself anymore, please contact me if you are interested in working on verification in the field of embedded software, preferably via email. We can probably find an interesting topic and a supervisor.

- **Ongoing**
- **Finished**

- Na Bai (Diploma): *Dataflow Analysis for PLCs (September 2011)*
- Sebastian Biallas (Diploma): *Counterexample-Guided Abstraction Refinement for Programmable Logic Controllers (April 2010)*
- Frank Birbacher (Diploma): *Relational Static Analysis of IL-Programs using Congruences*
- Lucas Brutschy (B.Sc.): *Static Analysis of Microcontroller Software using SAT- and Constraint-Solving (August 2009)*
- Mustafa Karafil (Diploma): *Recovering Indirect Control Flow in Binary Code (August 2011)*
- Jörg Toborg (Diploma): *Static Analysis for the Renesas R8C/23 Tiny Microcontroller (February 2010)*

## Publications

A more detailed list of my publications can be found [here](#) (including abstracts), and a list of my co-authors can be found [here](#).

[RBH+14]

[PDFBIB](#)

Reinbacher, T., Brauer, J., Horauer, M., Steininger, A., and Kowalewski, S., "Runtime verification of microcontroller binary code", *Science of computer programming*, vol. 80, pp. 109-129, 2014

## Runtime verification of microcontroller binary code

### Bibtex entry :

```
@article { RBH+14,  
  author = { Reinbacher, Thomas and Brauer, J{"o}rg and Horauer,  
  Martin  
    and Steininger, Andreas and Kowalewski, Stefan },  
  title = { Runtime verification of microcontroller binary code },  
  journal = { Science of computer programming },  
  publisher = { Elsevier },  
  pages = { 109-129 },  
  volume = { 80 },  
  year = { 2014 },  
  address = { Amsterdam },  
  issn = { 0167-6423 },  
  organization = { Brazilian Symposium on Programming Languages },  
  doi = { 10.1016/j.scico.2012.10.015 },  
  typ = { PUB:(DE-HGF)16 },  
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  cin = { 120000 / 122810 },  
  url = { http://publications.rwth-aachen.de/record/231479 },  
}
```

[RFB14]

[PDFBIB](#)

Reinbacher, T., Fuegger, M., and Brauer, J., "Runtime verification of embedded real-time systems", *Formal methods in system design*, vol. 44, iss. 3, pp. 203-239, 2014

# Runtime verification of embedded real-time systems

## Bibtex entry :

```
@article { RFB14,
  author = { Reinbacher, Thomas and Fuegger, Matthias and Brauer,
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  title = { Runtime verification of embedded real-time systems },
  journal = { Formal methods in system design },
  publisher = { Springer Science + Business Media B.V },
  pages = { 203-239 },
  volume = { 44 },
  number = { 3 },
  year = { 2014 },
  address = { Dordrecht },
  issn = { 0925-9856 },
  doi = { 10.1007/s10703-013-0199-z },
  typ = { PUB:(DE-HGF)16 },
  reportid = { RWTH-CONV-089599 },
  cin = { 120000 / 122810 },
  url = { http://publications.rwth-aachen.de/record/446689 },
}
```

[BK13]

[PDFBIB](#)

Brauer, J. and Kowalewski, S., "Automatic abstraction for bit vectors using decision procedures", Aachen, AIB 2013 14, 2013.

## Automatic abstraction for bit vectors using decision procedures

### Bibtex entry :

```
@techreport { BK13,
  author = { Brauer, J{\\"o}rg and Kowalewski, Stefan },
  title = { Automatic abstraction for bit vectors using decision
    procedures },
  publisher = { Fachgruppe Informatik, RWTH Aachen University },
  pages = { IV, 207 S. : graph. Darst. },
  volume = { 2013,14 },
  number = { AIB 2013 14 },
  series = { Aachener Informatik-Berichte },
  year = { 2013 },
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  typ = { PUB:(DE-HGF)11 },
  reportid = { RWTH-CONV-010470 },
  cin = { 120000 / 122810 },
  url = {
    http://publications.rwth-aachen.de/record/229199/files/4836.pdf },
}
```

```
}
```

[BKK13]

[PDFBIB](#)

Brauer, J., King, A., and Kowalewski, S., "Abstract interpretation of microcontroller code: Intervals meet congruences", *Science of computer programming*, vol. 78, iss. 7, pp. 862-883, 2013

## Abstract interpretation of microcontroller code: Intervals meet congruences

**Bibtex entry :**

```
@article { BKK13,  
  author = { Brauer, J{"o}rg and King, Andy and Kowalewski, Stefan  
},  
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  pages = { 862-883 },  
  volume = { 78 },  
  number = { 7 },  
  year = { 2013 },  
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  url = { http://publications.rwth-aachen.de/record/238031 },  
}
```

[KPB13]

[PDFBIB](#)

Kowalewski, S., Philippou, A., and Brauer, J., "Model checking and abstract interpretation as building blocks of advanced program analysis techniques", *International journal on software tools for technology transfer : STTT*, vol. 15, iss. 4, pp. 287-289, 2013

## Model checking and abstract interpretation as building blocks of advanced program analysis techniques

**Bibtex entry :**

```
@article { KPB13,  
  author = { Kowalewski, Stefan and Philippou, A. and Brauer, J. },
```

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title = { Model checking and abstract interpretation as building
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journal = { International journal on software tools for technology
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publisher = { Springer },
pages = { 287-289 },
volume = { 15 },
number = { 4 },
year = { 2013 },
address = { Berlin ; Heidelberg [u.a.] },
issn = { 1433-2787 },
organization = { 15. International Conference, TACAS 2009, York
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doi = { 10.1007/s10009-013-0280-3 },
typ = { PUB:(DE-HGF)16 },
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}

```

[BBK+12]

[PDFBIB](#)

Biallas, S., Brauer, J., King, A., and Kowalewski, S., "Loop Leaping with Closures", in *Proc. Static Analysis : 19th International Symposium, SAS 2012, Deauville, France, September 11-13, 2012. Proceedings / edited by Antoine Miné, David Schmidt*, Berlin, Heidelberg, 2012 in *Lecture Notes in Computer Science*, Springer, pp. 214-230.

## Loop Leaping with Closures

### Bibtex entry :

```

@inproceedings { BBK+12,
  author = { Biallas, Sebastian and Brauer, J{"o"}rg and King, Andy
and
            Kowalewski, Stefan },
  title = { Loop Leaping with Closures },
  booktitle = { Static Analysis : 19th International Symposium, SAS
2012,
              Deauville, France, September 11-13, 2012. Proceedings /
              edited by Antoine Miné, David Schmidt },
  publisher = { Springer },
  pages = { 214-230 },
  series = { Lecture Notes in Computer Science },
  year = { 2012 },
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cin = { 122810 / 120000 },  
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[BBK12a]

[PDFBIB](#)

Beckschulze, E., Brauer, J., and Kowalewski, S., "Access-Based Localization for Octagons", *Electronic notes in theoretical computer science : ENTCS*, vol. 287, pp. 29-40, 2012

## Access-Based Localization for Octagons

### Bibtex entry :

```
@article { BBK12a,  
  author = { Beckschulze, Eva and Brauer, J{"o}rg and Kowalewski,  
Stefan },  
  title = { Access-Based Localization for Octagons },  
  journal = { Electronic notes in theoretical computer science :  
ENTCS },  
  publisher = { Elsevier Science },  
  pages = { 29-40 },  
  volume = { 287 },  
  year = { 2012 },  
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  organization = { 4. International Workshop on Numerical and  
Symbolic Abstract  
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  url = { http://publications.rwth-aachen.de/record/165238 },  
}
```

[BBK12b]

[PDFBIB](#)

Biallas, S., Brauer, J., and Kowalewski, S., "Arcade.PLC : a Verification Platform for Programmable Logic Controllers", in *Proc. 2012 proceedings of the 27th IEEE/ACM International Conference on Automated Software Engineering (ASE 2012) : Essen, Germany, 3 - 7 September 2012*, Piscataway, NJ, 2012, IEEE, pp. 338-341.

## Arcade.PLC : a Verification Platform for Programmable Logic Controllers

### Bibtex entry :

```
@inproceedings { BBK12b,  
  author = { Biallas, Sebastian and Brauer, J{"o}rg and Kowalewski,  
Stefan },  
  title = { Arcade.PLC : a Verification Platform for Programmable
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Logic
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booktitle = { 2012 proceedings of the 27th IEEE/ACM International
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publisher = { IEEE },
pages = { 338-341 },
year = { 2012 },
address = { Piscataway, NJ },
organization = { 27. IEEE/ACM International Conference on Automated
Software
    Engineering, Essen (Germany), 2012-09-03 - 2012-09-07 },
doi = { 10.1145/2351676.2351741 },
typ = { PUB:(DE-HGF)8 },
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cin = { 120000 / 122810 },
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```

[BHK+12]

[PDFBIB](#)

Brauer, J., Hansen, R. R., Kowalewski, S., Larsen, K. G., and Olesen, M. C., "Adaptable Value-Set Analysis for Low-Level Code", in *Proc. 6th International Workshop on Systems Software Verification (SSV 2011) [Elektronische Ressource] / Hrsg.: Jörg Brauer ; Marco Roveri ; Hendrik Tews*, Wadern, 2012 in OASICS - OpenAccess Series in Informatics, Schloss Dagstuhl - Leibniz-Zentrum für Informatik, pp. 32-43.

## Adaptable Value-Set Analysis for Low-Level Code

### Bibtex entry :

```

@inproceedings { BHK+12,
    author = { Brauer, J{"o}rg and Hansen, Rene Rydhof and Kowalewski,
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    title = { Adaptable Value-Set Analysis for Low-Level Code },
    booktitle = { 6th International Workshop on Systems Software
Verification
        (SSV 2011) [Elektronische Ressource] / Hrsg.: J{"o}rg
        Brauer ; Marco Roveri ; Hendrik Tews },
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},
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url = { http://publications.rwth-aachen.de/record/128784 },  
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[BK12a]

[PDFBIB](#)

Brauer, J. and King, A., "Transfer function synthesis without quantifier elimination", *Logical methods in computer science : LMCS*, vol. 8, iss. 3, 2012

## Transfer function synthesis without quantifier elimination

### Bibtex entry :

```
@article { BK12a,  
  author = { Brauer, J{\\"o}rg and King, Andy },  
  title = { Transfer function synthesis without quantifier  
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  publisher = { Department of Theoretical Computer Science, TU [u.a.]  
},  
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  cin = { 120000 / 122810 },  
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http://publications.rwth-aachen.de/record/218122/files/218122.pdf },  
}
```

[BS12]

[PDFBIB](#)

Brauer, J. and Simon, A., "Inferring Definite Counterexamples Through Under-Approximation", in *Proc. NASA formal methods : 4th international symposium, NFM 2012, Norfolk, VA, USA, April 3 - 5, 2012 ; proceedings / Alwyn E. Goodloe; Suzzette Person (ed.)*, Berlin ; Heidelberg [u.a.], 2012 in Lecture Notes in Computer Science, Springer, pp. 54-69.

## Inferring Definite Counterexamples Through Under-Approximation

### Bibtex entry :

```
@inproceedings { BS12,  
  author = { Brauer, J{\\"o}rg and Simon, Axel },  
  title = { Inferring Definite Counterexamples Through  
Under-Approximation },
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booktitle = { NASA formal methods : 4th international symposium,
NFM 2012,
    Norfolk, VA, USA, April 3 - 5, 2012 ; proceedings / Alwyn E.
    Goodloe; Suzette Person (ed.) },
publisher = { Springer },
pages = { 54-69 },
series = { Lecture Notes in Computer Science },
year = { 2012 },
address = { Berlin ; Heidelberg [u.a.] },
organization = { NASA formal methods : 4. international symposium,
Norfolk,
    VA (USA), 2012-04-03 - 2012-04-05 },
typ = { PUB:(DE-HGF)8 },
reportid = { RWTH-CONV-194497 },
cin = { 122810 / 120000 },
url = { http://publications.rwth-aachen.de/record/123648 },
}

```

[BSK12]

[PDFBIB](#)

Brauer, J., Schlich, B., and Kowalewski, S., "Parallel and distributed invariant checking of microcontroller software", *Electronic notes in theoretical computer science : ENTCS*, vol. 287, pp. 45-63, 2012

## Parallel and distributed invariant checking of microcontroller software

### Bibtex entry :

```

@article { BSK12,
    author = { Brauer, J{"o}rg and Schlich, Bastian and Kowalewski,
Stefan },
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ENTCS },
    publisher = { Elsevier Science },
    pages = { 45-63 },
    volume = { 287 },
    year = { 2012 },
    address = { Amsterdam [u.a.] },
    issn = { 1571-0661 },
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Symbolic Abstract
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    doi = { 10.1016/j.entcs.2009.09.059 },
    typ = { PUB:(DE-HGF)16 },
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    cin = { 122810 / 120000 },
    url = { http://publications.rwth-aachen.de/record/132534 },
}

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}

[BBK+11]

[PDFBIB](#)

Biallas, S., Brauer, J., Kowalewski, S., and Schlich, B., "Automatically Deriving Symbolic Invariants for PLC Programs Written in IL", in *Proc. Formal methods for automation and safety in railway and automotive systems : FORMS/FORMAT 2010 ; [8th symposium ; proceedings] / Ekehard Schnieder; Géza Tarnai, eds.*, Heidelberg [u.a.], 2011, Springer, pp. 237-245.

## Automatically Deriving Symbolic Invariants for PLC Programs Written in IL

**Bibtex entry :**

```
@inproceedings { BBK+11,  
  author = { Biallas, Sebastian and Brauer, J{"o}rg and Kowalewski,  
    Stefan and Schlich, Bastian },  
  title = { Automatically Deriving Symbolic Invariants for PLC  
Programs  
Written in IL },  
  booktitle = { Formal methods for automation and safety in railway  
and  
automotive systems : FORMS/FORMAT 2010 ; [8th symposium ;  
proceedings] / Ekehard Schnieder; Géza Tarnai, eds. },  
  publisher = { Springer },  
  pages = { 237-245 },  
  year = { 2011 },  
  address = { Heidelberg [u.a.] },  
  organization = { Formal methods for automation and safety in  
railway and  
automotive systems, 2010 },  
  doi = { 10.1007/978-3-642-14261-1 },  
  typ = { PUB:(DE-HGF)8 },  
  reportid = { RWTH-CONV-196797 },  
  cin = { 122810 / 120000 },  
  url = { http://publications.rwth-aachen.de/record/126461 },  
}
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[BBK11]

[PDFBIB](#)

Biallas, S., Brauer, J., and Kowalewski, S., "SAT-Based Abstraction Refinement for Programmable Logic Controllers", in *Proc. 3rd International Workshop on Dependable Control of Discrete Systems 2011, DCDS 2011, Saarbrücken, Germany, 15th-17th June 2011*, Piscataway, NJ, 2011, IEEE, pp. 96-101.

## SAT-Based Abstraction Refinement for Programmable Logic Controllers

**Bibtex entry :**

```
@inproceedings { BBK11,
  author = { Biallas, Sebastian and Brauer, J{"o}rg and Kowalewski,
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  title = { SAT-Based Abstraction Refinement for Programmable Logic
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  booktitle = { 3rd International Workshop on Dependable Control of
Discrete
    Systems 2011, DCDS 2011, Saarbr{"u}cken, Germany,
    15th-17thJune 2011 },
  publisher = { IEEE },
  pages = { 96-101 },
  year = { 2011 },
  address = { Piscataway, NJ },
  organization = { 3. International Workshop on Dependable Control of
Discrete
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}
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[BBS+11]

[PDFBIB](#)

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## Analyzing Embedded Systems Code for Mixed-Critical Systems Using Hybrid Memory Representations

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```
@inproceedings { BBS+11,
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[BK11]

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### Bibtex entry :

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@inproceedings { BK11,
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@inproceedings { BK11a,
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Saarbr{"u}cken
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  url = { http://publications.rwth-aachen.de/record/126458 },
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### Bibtex entry :

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@inproceedings { BKK11,
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title = { Existential Quantification as Incremental SAT },
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url = { http://publications.rwth-aachen.de/record/126209 },
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@techreport { BRT11,
author = { Brauer, J{\o}rg and Roveri, Marco and Tews, Hendrik },
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[RB11]

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@inproceedings { RB11,  
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[RBH+11]

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[RBS+11]

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  author = { Reinbacher, Thomas and Brauer, J{"o}rg and Schachinger,
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  booktitle = { Runtime Verification : Second International
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url = { http://publications.rwth-aachen.de/record/123647 },
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@inproceedings { RSM+11,  
  author = { Reinbacher, Thomas and Steininger, Andreas and  
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  title = { Hardware Support for Efficient Testing of Embedded  
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    Technical Conferences and Computers and Information in  
    Engineering Conference - 2011 : presented at ASME 2011  
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    28 - 31, 2011, Washington, D.C. / sponsored by the Design  
    Engineering Division, ASME; the Computers and Information in  
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Conferences  
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[SBK11]

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@article { SBK11,
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International Haifa Verification Conference, HCV 2009,
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[BBG+10]

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  author = { Biallas, Sebastian and Brauer, J{"o}rg and G{"u}ckel,
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[BK10]

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@inproceedings { BK10,
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2010,
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series = { Lecture notes in computer science },
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url = { http://publications.rwth-aachen.de/record/119140 },
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[BKK+10]

[PDFBIB](#)

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### Bibtex entry :

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@inproceedings { BKK+10,
author = { Brauer, J{\o}rg and Kamin, Volker and Kowalewski,
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booktitle = { SSV'10 : Proceedings of the 5th international
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year = { 2010 },
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verification },
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}
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  international workshop, Antwerp (Belgium), 2010-09-20 -
  2010-09-21 },
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  url = { http://publications.rwth-aachen.de/record/119141 },
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[BNS10]

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url = { http://publications.rwth-aachen.de/record/120063 },  
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[GBK10]  
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### Bibtex entry :

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  Binary Code Verification },  
  booktitle = { 2010 International Symposium on Industrial Embedded  
Systems  
(SIES 2010) : Trento, Italy, 7 - 9 July 2010 / [University  
of Trento, Italy; IEEE; IES] },  
  publisher = { IEEE },  
  pages = { 118-127 },  
  year = { 2010 },  
  address = { Piscataway, NJ },  
  organization = { 2010 International Symposium on Industrial  
Embedded Systems,  
  Trento (Italy), 2010-07-07 - 2010-07-09 },  
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cin = { 122810 / 120000 },
url = { http://publications.rwth-aachen.de/record/119226 },
}

```

[GSB+10]

[PDFBIB](#)

Gückel, D., Schlich, B., Brauer, J., and Kowalewski, S., "Synthesizing Simulators for Model Checking Microcontroller Binary", in *Proc. Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14–16, 2010, Vienna, Austria / Sponsored by IEEE Computer Society, Test Technology Techn. Council, In coop. with Dept. of Computer Engineering, Fac. of Informatics, Vienna Univ. of Techn., Piscataway, NJ, 2010, IEEE*, pp. 313-316.

## Synthesizing Simulators for Model Checking Microcontroller Binary

### Bibtex entry :

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@inproceedings { GSB+10,
  author = { G{"u"}ckel, Dominique and Schlich, Bastian and Brauer,
    J{"o"}rg and Kowalewski, Stefan },
  title = { Synthesizing Simulators for Model Checking
Microcontroller
  Binary },
  booktitle = { Proceedings of the 13th IEEE Symposium on Design and
Diagnostics of Electronic Circuits and Systems : April
14–16, 2010, Vienna, Austria / Sponsored by IEEE Computer
Society, Test Technology Techn. Council, In coop. with Dept.
of Computer Engineering, Fac. of Informatics, Vienna Univ.
of Techn. },
  publisher = { IEEE },
  pages = { 313-316 },
  year = { 2010 },
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  organization = { 13. IEEE Symposium on Design and Diagnostics of
Electronic
Circuits and Systems, Vienna (Austria), 2010-04-14 -
2010-04-16 },
  doi = { 10.1109/DDECS.2010.5491761 },
  typ = { PUB:(DE-HGF)8 },
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  url = { http://publications.rwth-aachen.de/record/119227 },
}

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[RBH+10]

[PDFBIB](#)

Reinbacher, T., Brauer, J., Horauer, M., Steininger, A., and Kowalewski, S., "Test-Case Generation for Embedded Binary Code Using Abstract Interpretation", in *Proc. Sixth Doctoral Workshop on Mathematical and Engineering Methods in Computer Science (Selected Papers)*

(MEMICS 2010) [Elektronische Ressource] / Hrsg.: Ludek Matyska ; Michal Kozubek ; Tomáš Vojnar ; Pavel Zemčík ; David Antos, Wadern, 2010 in OASICS - OpenAccess Series in Informatics, Schloss Dagstuhl - Leibniz-Zentrum für Informatik, pp. 101-108.

## Test-Case Generation for Embedded Binary Code Using Abstract Interpretation

### Bibtex entry :

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@inproceedings { RBH+10,  
  author = { Reinbacher, Thomas and Brauer, Jörg and Horauer,  
  Martin  
    and Steininger, Andreas and Kowalewski, Stefan },  
  title = { Test-Case Generation for Embedded Binary Code Using  
  Abstract  
  Interpretation },  
  booktitle = { Sixth Doctoral Workshop on Mathematical and  
  Engineering  
  Methods in Computer Science (Selected Papers) (MEMICS 2010)  
  [Elektronische Ressource] / Hrsg.: Ludek Matyska ; Michal  
  Kozubek ; Tomáš Vojnar ; Pavel Zemčík ; David Antos },  
  publisher = { Schloss Dagstuhl - Leibniz-Zentrum für Informatik  
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  pages = { 101-108 },  
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  year = { 2010 },  
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[BHS09]

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Brauer, J., Huuck, R., and Schlich, B., "Interprocedural pointer analysis in Goanna", *Electronic notes in theoretical computer science : ENTCS*, vol. 254, pp. 65-83, 2009

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### Bibtex entry :

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@article { BHS09,  
  author = { Brauer, Jörg and Huuck, Ralf and Schlich, Bastian },  
  title = { Interprocedural pointer analysis in Goanna },  
  journal = { Electronic notes in theoretical computer science :
```

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ENTCS },
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  pages = { 65-83 },
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  year = { 2009 },
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  issn = { 1571-0661 },
  doi = { 10.1016/j.entcs.2009.09.060 },
  typ = { PUB:(DE-HGF)16 },
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  cin = { 122810 / 120000 },
  url = { http://publications.rwth-aachen.de/record/132532 },
}
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[BSR+09]

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## Stack bounds analysis of microcontroller assembly code

### Bibtex entry :

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@inproceedings { BSR+09,
  author = { Brauer, J{\o}rg and Schlich, Bastian and Reinbacher,
Thomas
  and Kowalewski, Stefan },
  title = { Stack bounds analysis of microcontroller assembly code },
  booktitle = { Embedded Systems Week 2009 : CODES+ISSS'09, CASES'09,
EMSOFT'09 ; Proceedings of the 2009 international
  conference on Compilers, architecture, and synthesis for
  embedded systems ; 2009, Grenoble, France, October 11 - 16,
  2009 },
  publisher = { ACM Press },
  year = { 2009 },
  address = { New York, NY },
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architecture,
  and synthesis for embedded systems, Grenoble (France),
  2009-10-11 - 2009-10-16 },
  doi = { 10.1145/1631716.1631721 },
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[RBH+09]



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# Refining assembly code static analysis for the Intel MCS-51 microcontroller

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@inproceedings { RBH+09,  
  author = { Reinbacher, Thomas and Brauer, J{"o"}rg and Horauer,  
  Martin  
    and Schlich, Bastian },  
  title = { Refining assembly code static analysis for the Intel  
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  booktitle = { 2009 IEEE International Symposium on Industrial  
  Embedded  
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  publisher = { IEEE },  
  pages = { 161-170 },  
  year = { 2009 },  
  address = { Piscataway, NJ },  
  organization = { 2009 IEEE International Symposium on Industrial  
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  url = { http://publications.rwth-aachen.de/record/99425 },  
}
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[RHS+09]

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Reinbacher, T., Horauer, M., Schlich, B., Brauer, J., and Scheuer, F., "Model checking assembly code of an industrial knitting machine", in *Proc. Proceedings of the 2009 Fourth International Conference on Embedded and Multimedia Computing : EM-Com 2009 : [December 10-12, 2009, Jeju Island, Korea]*, Piscataway, NJ, 2009, IEEE, p. 8.

# Model checking assembly code of an industrial knitting machine

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@inproceedings { RHS+09,
  author = { Reinbacher, Thomas and Horauer, Martin and Schlich,
  Bastian
    and Brauer, J{"o}rg and Scheuer, Florian },
  title = { Model checking assembly code of an industrial knitting
  machine },
  booktitle = { Proceedings of the 2009 Fourth International
  Conference on
    Embedded and Multimedia Computing : EM-Com 2009 : [December
    10-12, 2009, Jeju Island, Korea] },
  publisher = { IEEE },
  pages = { 8 S. },
  year = { 2009 },
  address = { Piscataway, NJ },
  organization = { 2009 Fourth International Conference on Embedded
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    Multimedia Computing, Jeju Island (South Korea), 2009-12-10
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  url = { http://publications.rwth-aachen.de/record/129021 },
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[SBW+09]

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Schlich, B., Brauer, J., Wernerus, J., and Kowalewski, S., "Direct Model Checking of PLC Programs in IL", *IFAC Proceedings Volumes*, vol. 42, iss. 5, pp. 28-33, 2009

**Direct Model Checking of PLC Programs in IL****Bibtex entry :**

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@article { SBW+09,
  author = { Schlich, Bastian and Brauer, J{"o}rg and Wernerus,
  J{"o}rg
    and Kowalewski, Stefan },
  title = { Direct Model Checking of PLC Programs in IL },
  journal = { IFAC Proceedings Volumes },
  publisher = { Elsevier },
  pages = { 28-33 },
  volume = { 42 },
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  year = { 2009 },
  address = { Amsterdam },
  issn = { 1474-6670 },
  isbn = { 978-3-902661-44-9 },
  organization = { 2. IFAC Workshop on Dependable Control of Discrete
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Systems,  
    Bari (Italy), 2009-06-10 - 2009-06-12 },  
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    url = {  
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[HFS+08]

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## Goanna: syntactic software model checking

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@inproceedings { HFS+08,  
    author = { Huuck, Ralf and Fehnker, Ansgar and Seefried, Sean and  
    Brauer, J{\\"o}rg },  
    title = { Goanna: syntactic software model checking },  
    booktitle = { Automated technology for verification and analysis :  
6th  
    international symposium, ATVA 2008, Seoul, Korea, October 20  
    - 23, 2008 ; proceedings / Sungdeok (Steve) Cha; Jin-Young  
    Choi; Moonzoo Kim; Insup Lee; Mahesh Viswanathan (eds.) },  
    publisher = { Springer },  
    pages = { 216-221 },  
    series = { Lecture notes in computer science },  
    year = { 2008 },  
    address = { Berlin [u.a.] },  
    organization = { 6. International Symposium on Automated Technology  
for  
    Verification and Analysis, Seoul (South Korea), 2008-10-20 -  
    2008-10-23 },  
    doi = { 10.1007/978-3-540-88387-6_17 },  
    typ = { PUB:(DE-HGF)7 },  
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}
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## Invited Talks

- Existential Quantification as Incremental SAT. Technical University of Denmark, Copenhagen. 10-06-2011.
- Automatic Abstraction for Binary Code Verification. Aalborg University, Denmark. 13-04-2011.
- Automatic Abstraction for Intervals using Boolean Formula. Technical University of Munich, Germany. 14-05-2010.
- Static Analysis in [mc]square. University of Applied Sciences FH Technikum Vienna, Austria. 31-03-2009.

## Teaching

- Winter semester 2010/2011
  - [Formal Methods for Embedded Systems](#) (Lecture)
- Summer semester 2010
  - [Seminar: Programmanalyse](#) (Seminar)
- Winter semester 2009/2010
  - [Formal Methods for Embedded Systems](#) (Lecture)
  - [Verification and Program Analysis](#) (Seminar)
- Summer semester 2009
  - [Applying Formal Verification Methods to Embedded Systems](#) (Seminar)
- Winter semester 2008/2009
  - [Static Analysis of Embedded Systems Software](#) (Seminar)

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